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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,748	02/13/2004	Toshiyuki Furuie	248812US2	5312

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,748	FURUIE ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-13,15 and 16* is/are rejected.

7)☒ Claim(s) *2,3 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-16 are objected to because of the following informalities:

Claim 1, line 1, "for a semiconductor device" should be deleted.

Claim 1, line 5, "applying as said" should be changed to --applying said--.

Claim 1, line 5, "voltage a" should be changed to --voltage as a --.

Claim 1, line 9, "controller so controls" should be changed to --controller controls--.

Claim 1, line 9, "driver that" should be changed to --driver so that--.

Claims 2-9 are objected to because they include the informalities of claim 1.

Claim 2, line 2, "applying as said" should be changed to --applying said--.

Claim 2, line 2, "voltage a" should be changed to --voltage as a --.

Claim 2, line 5, "controller so controls" should be changed to --controller controls--.

Claim 2, line 5, "driver that" should be changed to --driver so that--.

Claim 6, line 2, "the maximum" should be changed to --a maximum-- to avoid lacks antecedent basis.

Claim 7, line 2, "the average" should be changed to --an average-- to avoid lacks antecedent basis.

Claim 7, line 4, "average to be" should be changed to --average of said main current to be--.

Claim 10, line 1, "for a semiconductor device" should be deleted.

Claims 11-16 are objected to because they include the informalities of claim 10.

Claim 13, line 2, "the maximum" should be changed to --a maximum-- to avoid lacks antecedent basis.

Claim 14, line 2, "the average" should be changed to --an average-- to avoid lacks antecedent basis.

Claim 14, line 4, "average to be" should be changed to --average of said main current to be--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 4-9, the recitation "said gate voltage" in these claims (line 2 of claims 4, 5, 8 and 9, and line 3 of claims 6 and 7) causes these claims to be indefinite since the fact that the voltage supply unit generates "said gate voltage" appears to be misdescriptive because it is inconsistent with what is recited earlier in claim 3. Note that claim 3 clearly recited that the voltage supply unit generates said third gate voltage, so it appears that "said gate voltage" in claims 4-9 (line 2 of claims 4, 5, 8 and 9, and line 3 of claims 6 and 7) should be changed to --said third gate voltage--. Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Igarashi (USP 6,057,728).

With respect to claim 1, Figure 2 of Igarashi disclose a drive circuit for driving an insulated gate transistor (1), which includes: a driver (7c, 7d) for applying a gate voltage (at node N1) to the transistor (1); and a timing controller for controlling timing (7a, 7b) of the driver (7c, 7d); wherein the driver (7c, 7d) is capable of applying the gate voltage (at node N1) as a first gate voltage (ground, when 7d is ON) which is lower than a threshold voltage of the transistor (1), and a second gate voltage (voltage supplied to 7c, when 7c is ON) which is a specific voltage for driving the transistor (1), and the functional recitation that the timing controller (7a, 7b) controls the driver (7c, 7d) so that application of the first gate voltage precedes application of the second gate voltage is also met in the operation of circuitry in Figure 2.

With respect to claim 10, Figure 2 of Igarashi discloses a drive circuit for driving an insulated gate transistor (1), which includes: a voltage supply unit (unit generated power supply Vcc to driver 7c-7d) for generate a gate voltage (voltage Vcc applied to 7c) to be applied to the transistor (1, at node N1) on the basing of a main current of the transistor (current at the gate and/or current at the source of transistor 1); a driver circuit (7c, 7d); and a timing controller (7a, 7b) for controlling timing of application of said gate voltage by said driver (7c, 7d).

6. Claims 1, 10-13, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Takizawa et al. (USP 5,926,012).

With respect to claim 1, Figure 15 of Takizawa et al. disclose a drive circuit for driving an insulated gate transistor (1), which includes: a driver (the resistors and bipolar transistors that are serially connected between supplies 36 and 37) for applying a gate voltage (at the base of 1) to the transistor (1); and a timing controller for controlling timing (whichever unit that is used to provided input signal to the bases of the bipolar transistors of the driver) of the driver (the resistors and bipolar transistors that are serially connected between supplies 36 and 37); wherein the driver (the resistors and bipolar transistors that are serially connected between supplies 36 and 37) is capable of applying the gate voltage (at base of 1) as a first gate voltage (ground/reference potential at the reference terminal of power supply 37) which is lower than a threshold voltage of the transistor (1), and a second gate voltage (voltage potential at the positive terminal of power supply 36) which is a specific voltage for driving the transistor (1), and the functional recitation that the timing controller controls the driver so that application of the first gate voltage precedes application of the second gate voltage is also met in the operation of circuitry in Figure 15.

With respect to claims 10-13, 15 and 16, Figure 15 of Takizawa et al. discloses a drive circuit for driving an insulated gate transistor (1), which includes: a voltage supply unit (36) for generate a gate voltage to be applied to the transistor (at the base of transistor 1) on the basing of a main current of the transistor (main current of transistor 1); a driver circuit (the resistors and bipolar transistors that are serially connected between supplies 36 and 37, and elements 33-35); and a timing controller (whichever unit that is used to provided input signal to the bases of the

bipolar transistors of the driver) for controlling timing of application of said gate voltage by said driver (the resistors and bipolar transistors that are serially connected between supplies 36 and 37). Note that the functional limitations of claims 11-13, 15 and 16 are met in the operation of the circuit in Figure 15 of Takizawa et al. because the structures of the claims are fully met. For example, the voltage unit generates the gate voltage based on the main current (i.e., current at the emitter of transistor 1 as the variable in generating the gate voltage) when the value of the emitter current of transistor 1 changes then the voltage of the emitter of transistor 1 also changes, and thus the gate voltage also changes (i.e., the emitter's voltage of transistor 1 increases gate voltage also increases), and the voltage supply unit also controls the gate voltage to allow slowdown in switching speed of the transistor when the main current is lower than a certain level (by the detection 31).

Allowable Subject Matter

7. Claims 1-9 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome and/or indefiniteness set forth above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER